REMARKS

The Office Action of **October 29, 2002** has been received and its contents carefully noted. Applicant respectfully submits that this response is timely filed and fully responsive to the Office Action.

Claims 1-12 and 34-74 were pending in the present application prior to the aforementioned amendment. By the above actions, claims 1, 3, 43, 45, 60 and 66 are amended to clarify the novel features of the present invention. Since these amendments are only merely further clarifying in nature, they should be considered acceptable after final rejection, since a new search should not be necessary. Accordingly, claims 1-12 and 34-74 are currently pending in the present application and, at least for the reasons set forth below, are believed to be in condition for allowance.

A. Claim Objections

The Examiner contends that, if claims 1 to 12 and 3-42 are found allowable, claims 43 to 49 will be objected to under 35 C.F.R. 1.75 as being substantial duplicates thereof. It should be noted, however, that independent claims 1 and 3 recite utilizing **both** the control gate electrode and a wiring for connecting the control gate electrode with the first signal line, while independent claims 43 and 45 recite only the control gate electrode without recitation of a wiring for connecting the control gate electrode with first signal line. Consequently, these claims are

sufficiently different from each other to be considered acceptable under 35 C.F.R. 1.75, and, thus, this objection should be reconsidered and withdrawn.

A. 35 U.S.C. §103 Rejection

Claims 1-12 and 34-42 stand rejected under 35 U.S.C. §103(a) as unpatentable over JP Patent No. 11-154714 to Yamazaki et al. (Hereinafter "Yamazaki") in view of U.S. Patent No. 5,656,845 to Akbar. It is respectfully contended that the claimed invention as presently amended clearly defines over the proposed combination of Yamazaki and Akbar for at least the following reasons.

The claimed invention is directed generally to nonvolatile memory including, *inter alia*, a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor.

Moreover, the nonvolatile memory in accordance with the rejected claims as presently amended requires:

(1) a first semiconductor active layer of the memory thin film transistor connected to a third signal line,

(2) a second semiconductor active layer of the switching thin film transistor connected to a fourth signal line,

(3) the second signal line be formed between the semiconductor active layers and the first signal line,

(4) the first signal line and the second signal line be perpendicular to the third signal line and the fourth signal line,

(5) formation of the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, and the first signal line and the second signal line of a same layer, and wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer, wherein at least two of the memory cells adjacent each other share the fourth signal line therebetween.

Applicant respectfully contends that Yamazaki, either alone or in combination with Akbar, clearly fails to expressly teach, disclose or inherently suggest each and every claim limitation of the prevent invention as presently amended. For the reasons advanced in the response of August 14, 2002, Applicants continue to believe that the presently claimed invention is patentably distinct over these cited references, the arguments advanced therein being incorporated herein by reference.

Moreover, each of the independent claims rejected under Section 103(a) are amended to recite that at least two of the recited memory cells adjacent to each other share the fourth signal line therebetween. This structure is supported by the specification of the instant application, at least, in Figure 8 and in Embodiment 4. With such a structure, the number of the fourth signal lines can be reduced as compared with the structure where a number of the memory cells adjacent to each are connected to different fourth signal lines as show in Figure 1. This permits the memory cells to be arranged at a higher density, which, in turn, can provide a nonvolatile memory having a reduced size or an increased capacity.

Neither Yamazaki nor Akbar appears to teach this additional feature of the present invention. As a result, any combination of these references will not be sufficient to teach or

suggest the presently claimed invention. Therefore, it is respectfully requested that the rejections based on Yamazaki and Akbar be reconsidered and withdrawn.

C. Non-Statutory Double Patenting Rejections

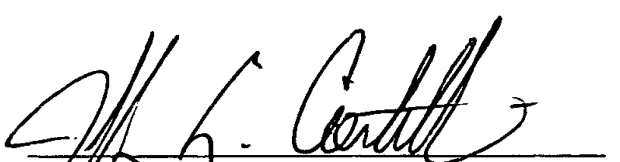
The Examiner provisionally rejects claims 1-12 and 34-74 under the judicially created doctrine of obviousness-type double patenting over claims 1-12 of copending U.S. Application No. 09/156,913, in view of Akbar and Yamazaki, and also over claims 1-30 of copending U.S. Application No. 09/988,729 in view of Akbar and Yamazaki et al. Applicant respectfully request that the Examiner hold these rejections in abeyance until an indication of allowance of the claims over the prior art has been indicated.

Conclusion

Accordingly, Applicant respectively submits that the pending claims are in proper condition for allowance and reconsideration and withdrawal of the pending rejections are requested.

If the Examiner believes further discussions with Applicant's representative would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,



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MARKED UP VERSION OF AMENDED CLAIMS

1. (Twice Amended) A nonvolatile memory comprising:

memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode;

a wiring for connecting the control gate electrode with a first signal line,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film;

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer, [and]

wherein the wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.

3. (Twice Amended) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode;

a wiring for connecting the control gate electrode with a first signal line,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film;

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is in a range of 1-100 nm while a second thickness of the second semiconductor active layer of the switching thin film transistor is in a range of 1-150 nm,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer, [and]

wherein the wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.

43. (Amended) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film; and

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor,

wherein the control gate electrode of the memory thin film transistor is connected to the first signal line,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer, [and]

wherein control gate electrode of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.

45. (Amended) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film; and

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is in a range of 1-100 nm while a second thickness of the second semiconductor active layer of the switching thin film transistor is in a range of 1-150 nm,

wherein the control gate electrode of the memory thin film transistor is connected to the first signal line,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer, [and]

wherein the control gate electrode of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.

60. (Amended) A semiconductor device comprising:

a memory cell array comprising a plurality of memory cells formed over a substrate in a matrix, each of the memory cells comprising:

a memory thin film transistor comprising a first semiconductor active layer formed on an insulating surface, a floating gate electrode and a first control gate electrode; and

a switching thin film transistor electrically connected to the memory thin film transistor, said switching thin film transistor comprising a second semiconductor active layer formed on the insulating surface and a second gate electrode,

a first signal line and a second signal line extending in parallel in a first direction over the substrate, said first signal line being electrically connected to the control gate electrode of the memory thin film transistor and said second signal line being electrically connected to the second gate electrode of the switching thin film transistor;

an interlayer insulating film formed over the first signal line and the second signal line;

a third signal line and a fourth signal line formed over the interlayer insulating film and extending in parallel in a second direction orthogonal to the first direction said third signal line being electrically connected to one of source and drain regions of the memory thin film transistor and said fourth signal line being electrically connected to one of source and drain regions of the switching thin film transistor; and

a conductive film formed over the interlayer insulating film, said conductive film electrically connecting said first signal line and said control gate electrode of the memory thin film transistor,

wherein the first semiconductor active layer and the second semiconductor active layer of one of the memory cells are formed in a common semiconductor island,

wherein the floating gate electrode of the memory thin film transistor, the second gate electrode of the switching thin film transistor, and the first and second signal lines are formed of a same layer,

wherein the third and fourth signal lines and said conductive film are formed of a same layer, [and]

wherein said conductive film extends across the second signal line, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.

66. (Amended) A semiconductor device comprising:

a display portion comprising a plurality of pixel thin film transistors over a substrate;

a memory cell array comprising a plurality of memory cells formed over a substrate in a matrix, each of the memory cells comprising:

a memory thin film transistor comprising a first semiconductor active layer formed on an insulating surface, a floating gate electrode and a first control gate electrode; and

a switching thin film transistor electrically connected to the memory thin film transistor, said switching thin film transistor comprising a second semiconductor active layer formed on the insulating surface and a second gate electrode;

a first signal line and a second signal line extending in parallel in a first direction over the substrate, said first signal line being electrically connected to the control gate electrode of the memory thin film transistor and said second signal line being electrically connected to the second gate electrode of the switching thin film transistor;

an interlayer insulating film formed over the first signal line and the second signal line;

a third signal line and a fourth signal line formed over the interlayer insulating film and extending in parallel in a second direction orthogonal to the first direction, said third signal line being electrically connected to one of source and drain regions of the memory thin film transistor and said fourth signal line being electrically connected to one of source and drain regions of the switching thin film transistor; and

a conductive film formed over the interlayer insulating film and electrically connecting said first signal line and said control gate electrode of the memory thin film transistor,

wherein the first semiconductor active layer and the second semiconductor active layer of one of the memory cells are formed in a common semiconductor island,

wherein the floating gate electrode of the memory thin film transistor, the second gate electrode of the switching thin film transistor, and the first and second signal lines are formed of a same layer,

wherein the third and fourth signal lines and said conductive film are formed of a same layer, [and]

wherein said conductive film extends across the second signal line, and

wherein at least two of the memory cells adjacent to each other share the fourth signal line therebetween.